IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of :

H. H. Chen, et al : Group Art No.: 2826

Serial No. 10/091,193 : Examiner: Tan Tran

Filed: March 5, 2002 : IBM Corporation
by Anne Vachon Dougherty
3173 Cedar Road
Yorktown Heights,
New York 10598

Title: SEMICONDUCTOR HIGH DIELECTRIC CONSTANT DECOUPLING CAPACITOR STRUCTURES AND PROCESS FOR FABRICATION

DECLARATION OF PRIOR INVENTION IN THE UNITED STATES TO OVERCOME CITED PATENT OR PUBLICATION (37CFR 1.131)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. This declaration is to establish completion of the invention in this application in the United States at a date prior to November 29, 1999, which is the earliest effective date of the U. S. Patent No. 6,265,280, entitled "Method for Manufacturing Cylindrical Semiconductor Capacitor" by Yang Pan, which was cited by the Examiner in the prosecution of the above-identified patent application.

2. The people making this declaration are two of the original joint inventors, Howard Hao Chen and Louis L. Hsu, who are present applicants for the pending patent application. The other applicant, Li-Kong Wang has retired and was not available to execute the Declaration.

3. To establish the date of completion of the invention of this application, the following attached document is submitted as evidence:

the invention disclosure submission form.

From this document, it can be seen that the invention in this application was made at least by the date November 28, 1999, which is a date earlier than the effective date of the cited reference.

Applicants aver that they were diligent in pursuing patent protection for the invention and that no unreasonable delay occurred from the time of submission of the invention disclosure to the original filing date for the parent patent application and have diligently pursued patent protection through to the present time.

Serial No. 10/091,193
Art Unit No. 2826

4. As a person signing below

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

Full name of first inventor: Howard Hao Chen

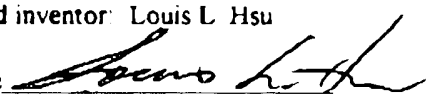
Inventor's signature_____

Date_____ Country of citizenship U. S.

Residence 2710 Evergreen Street, Yorktown Heights, New York 10598

Post Office Address same as above

Full name of second inventor: Louis L Hsu

Inventor's signature 

Date 9/18/03 Country of citizenship U. S.

Residence 7 Crosby Court, Fishkill, New York 12524

Post Office Address same as above

Y0999-420

Disclosure YOR8-1999-0162

Created By: Li-Kong Wang **Created On:** 02/12/99 09:56:42 AM
Last Modified By: Barbara Rasa **Last Modified On:** 03/08/99 10:23:05 AM

*** IBM Confidential ***

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

Summary

Status	Submitted
Processing Location	YOR
Functional Area	700 Systems, Technology & Science-Isaac
Attorney/Patent Professional	Kevin M Jordan/Watson/IBM
Submitted Date	03/05/99 12:20:19 PM
Owning Division	RES
PVT Score	48

Inventors with Lotus Notes ID's

Inventors: Howard Chen/Watson/IBM, Li-Kong Wang/Watson/IBM, Louis Hsu/Fishkill/IBM

Inventor Name > denotes primary contact	Inventor Serial	Div/Dept	Manager Serial	Manager Name
Chen, Howard H.	973821	22/KU8B	656952	Ling, David D.
> Wang, Li-Kong	669811	22/KUVC	308010	Emma, Philip G.
Hsu, LOUIS L.	713382	29/G9GA	793815	Wordeman, Matthew R. (Matt)

Inventors without Lotus Notes ID's

IDT Selection

IDT Team:	Attorney/Patent Professional:
	Kevin M Jordan/Watson/IBM

Main Idea

***Title of disclosure (in English)**

On Chip Ferroelectric Decoupling Capacitor

***Idea of disclosure**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

Ferroelectric Capacitor

The ferroelectric decoupling capacitors utilize the ferroelectric effect, which is the tendency of dipoles (small electrically asymmetric elements) within certain crystals to spontaneously polarize (align in parallel) under the influence of an externally applied electric field, and these elements remain polarized after the electric field is removed. Then reversing the electric field causes spontaneous polarization (i.e., alignment

of the dipoles) in the opposite direction. Thus, ferroelectric materials have two stable polarization states, and can be modeled as a bistable capacitor with two distinct polarization voltage thresholds. Since no external electric field or current is required for the ferroelectric material to remain polarized in either state, a capacitor can be built for storing charges that does not require power to retain the stored charges.

Ferroelectric (FE) films that are used as storage elements have relative dielectric constants which are a few orders of magnitude higher than that of silicon dioxide (e.g., 1000-1500 versus 3.8-7.0 of some typical DRAM capacitors). Thus a thicker film can be used to provide high capacitance. There are large number of ferroelectric materials available for thin film applications. Lead zirconnate titanate (PZT) has been most commonly used and studied. Thus we take this material as the example of capacitor material. A ferroelectric capacitor using lead zirconate titanate (PZT) film can store a larger charge, e.g., 10 uC/cm2 compared to an equivalent sized SiO2 capacitor that may store only 0.1 uC/cm2. Ferroelectric films such as the PZT remain ferroelectric from -80 to + 350°C, well beyond the operating temperature of existing silicon devices. Also, this FE film processing compatible with conventional semiconductor wafer processing techniques.

The earliest ferroelectric thin film is made of potassium nitrate and lead zirconate titanate (PZT). The storage capacitor was constructed from two metal electrodes thin FE film inserted between the metallization layers. Figure 1 shows a typical hysteresis I-V switching loop for the PZT film and operating characteristics.

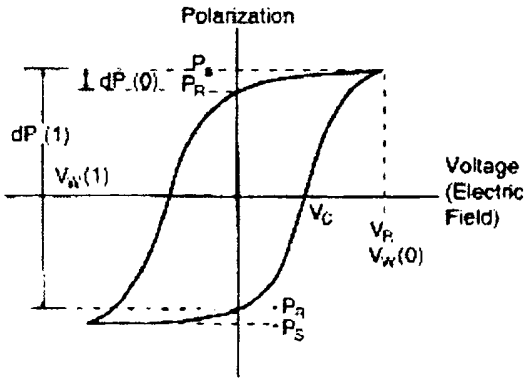


Figure 1. Schematic of a typical hysteresis curve of a ferroelectric capacitor.

For positive voltages greater than the coercive voltage (Vc)

applied to the ferroelectric capacitor, the film is polarized in the positive direction to a saturation value of Ps. The coercive voltage (Vc) is defined as the value where polarization reverses and the curve crosses the X-axis. On removal of the applied voltage, the polarization relaxes to a value Pr called the remnant polarization. On the application of negative voltage to the ferroelectric film, the resulting polarization is in the negative direction, reaching a saturation value of -Ps and a remnant (or relaxed) polarization of -Pr.

For a ferroelectric capacitor, once the capacitor is charged during the initial operation or the burn-in process with a voltage higher than Vr. The capacitor will remain at a capacitance value near the maximum capacitance even the power supply is removed. To change the direction of this polarization a negative voltage greater than -Vr has to apply to reverse the polarization. Thus the decoupling effect of the capacitor can be maintained even though without the power. This can effectively prevent any transient noise during the onset of the power supply.

Decoupling Capacitor

The decoupling capacitors has been widely used in the chip packaging to suppress the inductance induced transient current noise in the power supply lines. As described in the prior arts (1,2) the use of ferroelectric material capacitor in the packaging where noise has been a more series problem. However as the more recent chip technology pushes into higher speed, denser interconnects, and larger chip area the noise in the power supply lines due to circuit switching becomes a common problem for the chip applications. By adding the decoupling capacitors on the chip located in close proximity to the circuit can effectively reduce the power supply noise. In order to reduce the surge of noise to a desired level the value of this decoupling capacitance is typically 5 times of the line loading capacitance. Since these capacitors are fabricated in the same structure as the thin gate oxide transistors. the tradeoff between chip area, cost and reliability has to be considered greatly. In this invention disclosure we are proposing a compact size, high capacitance value and reliable capacitor using ferroelectric material which can be integrated into the silicon interconnect process easily with minimum added cost.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

Ferroelectric Decoupling Capacitor

Using the ferroelectric decoupling capacitor which can be fabricated between adjacent interconnect lines or between

interconnect lines of the same level can provide very large value of capacitance without any area or reliability penalty. In this invention disclosure we suggest a process method as well as a structure to implement this concept. The processing steps are described in figure 2 below.

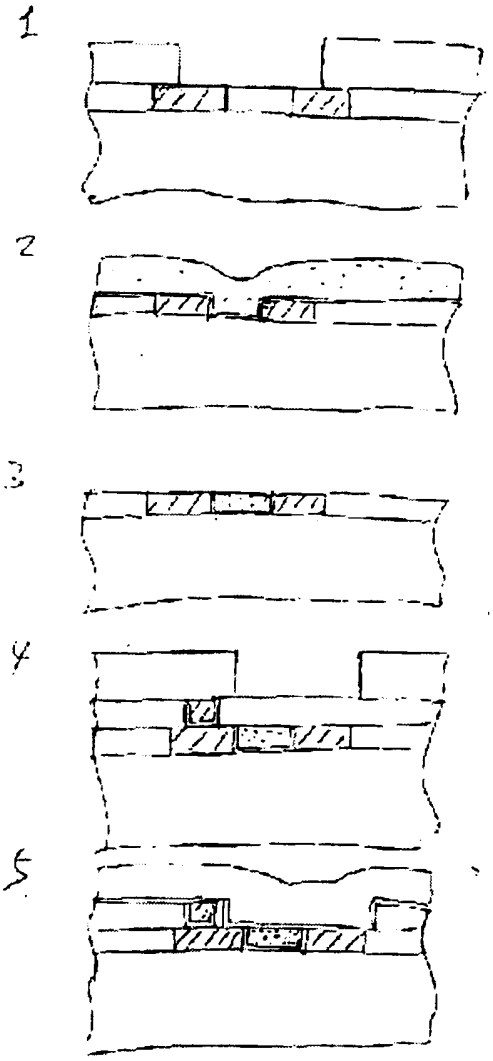


Figure 2 Process sequence of ferroelectric decoupling capacitors

1) Using a lithography and etching technique a window is opened on the lower level planarized interconnect. Subsequently the dielectric material between the two interconnect power (Vdd) and ground (Gnd) supply lines are removed using etching process.
2) The ferroelectric material is deposited and formed by

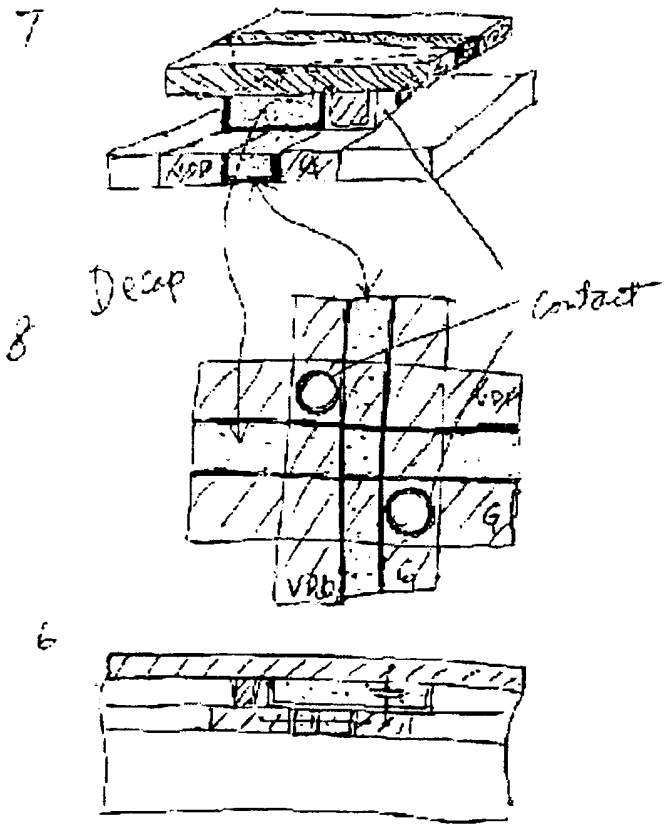
annealing process over the wafer. A barrier layer thin film is optional deposited prior to the ferroelectric thin film to prevent the reaction between the material of the interconnect and ferroelectric film chosen.

3) By using the planarization process, the ferroelectric material layer is removed except in the area between the two supply lines.

4) A dielectric film is deposited on the wafer and interconnect via is fabricated as normally done in the interconnect process.

5) The capacitor pattern area is opened to place the vertical capacitor. The process of this capacitor is the same as step 2.

6) The top layer of the interconnect metal layer is deposted and patterned which will connect to the metal line at the left side through the via contact and form the top electrode of the vertical ferroelectric capacitor on the right side metal line as shown in figure below.



This diagram (7) shows the final physical structure consists of the two types of decoupling capacitors. The capacitor between the adjacent power and ground lines can provide larger

capacitance but require more processing steps to fabricate. The capacitors between two levels of interconnects in the vertical direction can be easily fabricated and also does not require the power lines placed next to each other. The final diagram (8) shows the top view of the overall structure. The capacitors are fabricated both between the Vdd and Gnd line (lateral capacitors) and between interconnect layers (vertical capacitors).

In summary, we proposed to use ferroelectric material to fabricate the on-chip decoupling capacitors with two new structures and a processing technique to make those on-chip structures. This structure can be easily integrated into the existing semiconductor process with added benefits.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

Prior arts:
"Preparation and properties of sol-gel derived PZT thin films for decoupling capacitor application", Schwartz, R.W. Dimos, D. Lockwood, S.J. Torres, V.M., Integrated Ferroelectrics v.4 no.2 March 1994, pp.165-174.
"Electrical properties of sol-gel PZT thin films for decoupling capacitor applications", Schwartz, Robert W. Dimos, D. Lockwood, S.J. Torres, V.M., Ferroelectric Thin Films III Materials Research Society Symposium Proceedings v.310, 1993. pp.59-64.

These tow artical describe only capacitors used in the packaging. They are not on-chip thin film decoupling capacitors integrated into the interconnect structure.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

***Critical Questions (Questions 1 - 7 must be answered)**

***Question 1**
On what date was the invention workable? 03/01/99 **Please format the date as MM/DD/YYYY** (Workable means i.e. when you know that your design will solve the problem)

***Question 2**	
Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	
Are you aware of any publications, products or patents that relate to this invention?	○ Yes ● No